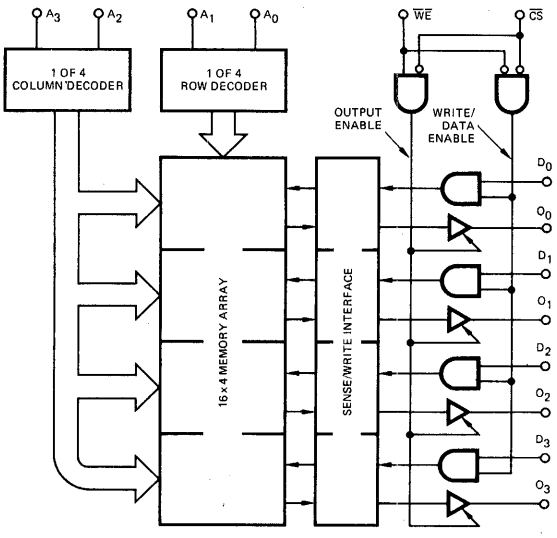
Am27S06 • Am27S07

Non-Inverting Schottky 64-Bit Random Access Memories

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit Low-power Schottky RAMs
- Ultra-high speed: Address access time typically 15ns
- Low Power: I_{CC} typically 75mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with three-state outputs (Am27S07) or with open collector outputs (Am27S06)
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for the assemblers of hybrid products

LOGIC BLOCK DIAGRAM



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ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collector Outputs		
Molded DIP	0°C to +75°C	AM27S06APC
Hermetic DIP	0°C to +75°C	AM27S06ADC
Hermetic DIP	–55°C to +125°C	AM27S06ADM
Hermetic Flat Pak	–55°C to +125°C	AM27S06AFM
Three-State Outputs		
Molded DIP	0°C to +75°C	AM27S07APC
Hermetic DIP	0°C to +75°C	AM27S07ADC
Hermetic DIP	–55°C to +125°C	AM27S07ADM
Hermetic Flat Pak	–55°C to +125°C	AM27S07AFM

FUNCTIONAL DESCRIPTION

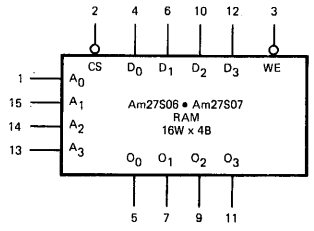
The Am27S06 and Am27S07 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am27S06) or three-state outputs (Am27S07). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW Write line $\overline{WE}$ controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four non-inverting outputs O_0 to O_3.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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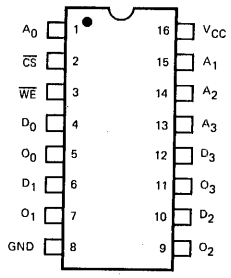
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	–0.5V to +7V
DC Voltage Applied to Outputs for High Output State	–0.5V to V_{CC} max.
DC Input Voltage	–0.5V to +5.5V
Output Current, Into Outputs	100mA
DC Input Current	–30mA to +5.0mA

OPERATING RANGE

Part No.	V_{CC}	Ambient Temperature
Commercial Grade Am27S06APC, DC Am27S07APC, DC	5.0V ±5%	0°C to +75°C
Military Grade Am27S06ADM, FM Am27S07ADM, FM	5.0V ±10%	–55°C to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	D. C. Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S07 Only)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –5.2mA I_{OH} = –2.0mA	COM'L MIL	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA I_{OL} = 20mA			0.350 0.380	0.45 0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.40V	$\overline{WE}$, D_0-D_3, A_0-A_3 $\overline{CS}$			–0.015 –0.030	.250 .250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				0.0	10	µA
I_{SC} (Am29701 Only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V			–20	–45	–90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		COM'L MIL		75 75	100 105	mA
V_C	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = –18mA				–0.850	–1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 2.4V		Am29700/01		0	40	µA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 0.4V, V_{CC} = MAX.		Am29701	–40	0		µA

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.

FUNCTION TABLE

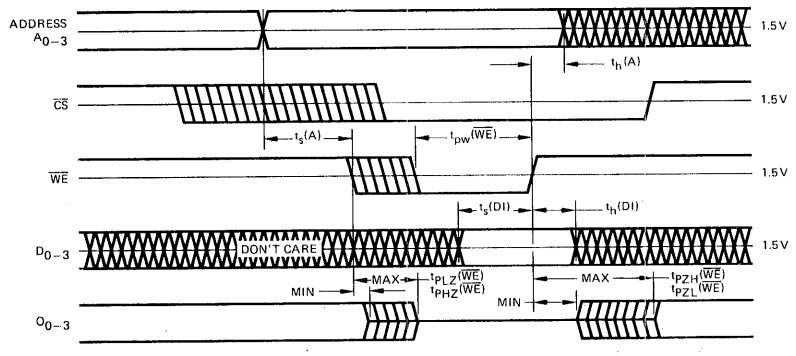
Input		Function	Data Output Status O_{0-3}
$\overline{CE}$	$\overline{WE}$		
Low	Low	Write	Output Disabled
Low	High	Read	Selected Word
High	Don't Care	Deselect	Output and Write Disabled

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description		A. C. Test Conditions	Typ. (Note 1)	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 2	Fig. 3 test load (measured to output = 1.5V)	22		35		50	ns
$t_{PZH}(\overline{CS})$ $t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 2		14		17		25	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2)	See Fig. 1		19		35		50	ns
$t_s(A)$	Set-up Time Address (Prior to Initiation of Write)	See Fig. 1		–6.0	0		0		ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 1		–2.5	0		0		ns
$t_s(DI)$	Set-up Time Data Input (Prior to Termination of Write)	See Fig. 1		18	25		25		ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 1		–4.0	0		0		ns
$t_{pw}(\overline{WE})$	Min. Write Enable Pulse Width to Insure Write	See Fig. 1		18	25		25		ns
$t_{PHZ}(\overline{CS})$ $t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)	See Fig. 2		13		17		25	ns
$t_{PLZ}(\overline{WE})$ $t_{PHZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 1		15		25		35	ns

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Output is preconditioned to data in during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch)

SWITCHING WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$ min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min. must be allowed before the address may be changed again. The output will be inactive (floating for the Am27S07) while the write enable is LOW.

Figure 1.

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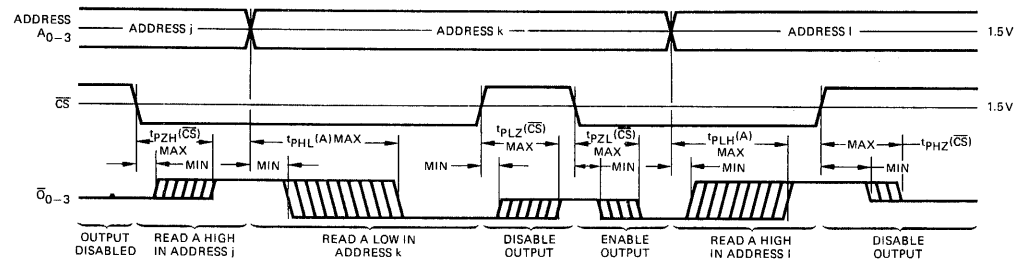
SWITCHING WAVEFORMS (Cont.)



Switching delays from address and chip select inputs to the data output. For the Am27S07 disabled output is "OFF", represented by a single center line. For the Am27S06, a disabled output is HIGH.

Figure 2.

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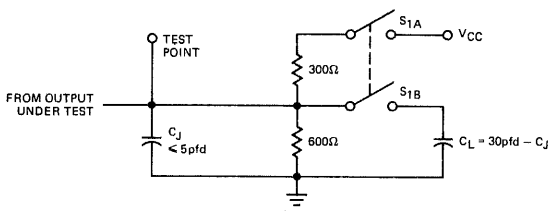
TEST LOAD

Open Collector Am27S06

S_1 is closed for all A. C. tests. Note that $t_{PHZ}(\overline{CS})$ and $t_{PHZ}(\overline{WE})$ parameters do not apply to 27S06 where disabled output is HIGH.



Three-State Am27S07

S_1 is closed for all A. C. tests except $t_{PHZ}(\overline{CS})$ and $t_{PHZ}(\overline{WE})$ where S_1 is open and jig capacitance (C_J) is $\leq$ 5pfd.

Figure 3.

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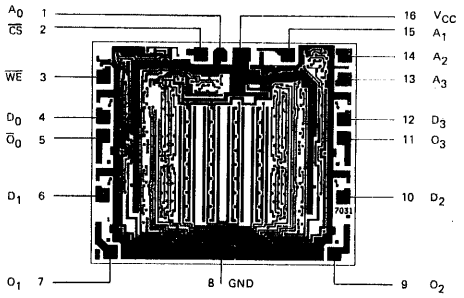
Metallization and Pad Layout



DIE SIZE
0.092" X 0.078"