



ND-100 OPERATOR'S COMMUNICATION INSTRUCTION SURVEY

ND-99.016.02 12/84

Further explanations found in ND-100 Reference Manual, ND-06.014

CONTROL FUNCTIONS (Do not affect DISPLAY)

System Control:

OPCOM	<input type="checkbox"/>		Enter Operator's Communication mode
		ESC key	Leave Operator's Communication mode
MCL	<input type="checkbox"/>	MACL	Generate Master Clear
STOP	<input type="checkbox"/>	STOP	Stop Program and enter OPCOM mode
LOAD	<input type="checkbox"/>	& or \$	Load according to ALD code (read by I12/)
		xxxxxx& or xxxxxx\$	Load from device x

Program Control:

		!	Continue program from address of program counter
xxxxxx!			Start program from address x
		Z	Execute a single instruction according to program counter
xxxxxxZ			Execute x instructions from address of program counter
xxxxxx.			Execute program until program counter = x and stop
		xxxxxx''	Execute Instruction Code x repeatedly
xxxxxx!O/nnnnnn			Execute IOX instruction with device number x

OPR = Output Data n = Returned Data

Miscellaneous Functions:

xxx#			Do Memory Test in segment x from address of B register to address of X register. P = Fail. Address, T = Fail. Bits, D = Fail. Pattern, L = Test Pattern.
space or @			Delete entry
*nnnnn			Current location of memory examine is n (16 least sign. bits)
OPR/nnnnnnzzzzzz			Change Operator's Panel Switches from n to z

OPR = Output Data n = Returned Data

DISPLAY FUNCTIONS (Affect only DISPLAY)

uuzzyxF \neq Define format of displayed information (F \neq is default)

x (3 bits): 0 = Octal
1 = Decoded according to z
2 = Binary

y (3 bits): 0 = Normal
1 = Stretch Zeros
2 = Stretch Ones
3 = Stretch Zeros and Ones

z (6 bits): Decode the 4 bits z to z+3 to a ONE among ZEROs.

u (4 bits): For Display Processor maintenance

1 = Display Year and Month
2 = Inhibit message
4 = Initialize panel processor
10 = Abort message

yxBUS/ Display Memory Accesses on ND-100 Bus

x (3 bits): 0 = Undefined
1 = Read Access
2 = Write Access
3 = Write or Read Access

y (3 bits): 0 = CPU Data
1 = DMA Data
2 = CPU Address
3 = DMA Address

ACT/ Display computer activity (default after MACL)

ND-100 INTERNAL REGISTERS AND THEIR BIT ASSIGNMENT

INTERNAL REGISTER NUMBER

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

[0] TRA PANS	PAN PRES	PAN FULL	READ	COM RDY	0	2	1	0	7	6	5	4	3	2	1	0	
					PCOM				RPAN								
[0] TRR PANC	0	0	READ	0	0	2	1	0	7	6	5	4	3	2	1	0	
					PCOM				WPAN								
[1] TRA STS	IONI	PONI	SEXI	N 100	3	2	1	0	M	C	O	Q	Z	K	TG	PTM	
[1] TRR STS	NOT ASSIGNED								M	C	O	Q	Z	K	TG	PTM	
[2] TRA OPR																	
[2] TRR LMP																	
[3] TRA PGS	FF	PM	NOT ASSIGNED						1	0	5	4	3	2	1	0	
					PT		VPN										
[3] TRR PCR	NOT ASSIGNED						1	0	1	0	3	2	1	0	0	1	0
	PT		APT		PIL						RING						
[4] TRA PVL	1	1	0	1	0	1	1	1	1	3	2	1	0	0	1	0	
	PREV. LEVEL																
[5] TRA IIC	NOT ASSIGNED											3	2	1	0		
												IIC CODE					
[5] TRR IIE	NOT ASSIGNED				POW	MOR	PTY	IOX	PI	Z	II	PF	MPV	MC	0		
[6] TRA/TRR PHD																	
[7] TRA/TRR PIE																	
[10] TRA CSR	NOT ASSIGNED												MAN DIS	CON	CUP		
[10] TRR CCLR	DATA LESS																
[11] TRR LCILR	N.A.	13													LOWER LIMIT PAGE NUMBER		0
[11] TRA ACTL																	
[12] TRA ALD	0	0	M	0	ADDRESS												
[12] TRR UCILR	N.A.	13													UPPER LIMIT PAGE NUMBER		0
[13] TRA PES	FETCH	DMA	FATAL	4	3	2	1	0	23	22	21	20	19	18	17	16	
	ERROR CODE								UPPER MEMORY ADDRESS								
[14] TRA 14 read paging control register	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0
	PT		APT		PIL						RING						
[15] TRA PEA	LOWER MEMORY ADDRESS																
[15] TRR ECCR	NOT ASSIGNED											TEST 6	DIS	ANY	TEST 15	TEST 0	

* Required level information in the A-register before the TRA instruction

N.A. = Not Assigned

Deposit Rules:

The contents are only changed by zzzzzz ⚡ in STOP mode, and by zzzzzzDEP ⚡ in STOP or RUN mode.

The contents are unchanged by ⚡ in STOP or RUN mode, and by zzzzzz ⚡ in RUN mode (? is answered).

Explanations:

- = Control Panel button
- ⚡ = Carriage Return
- n = Computer answer

All other characters are typed by the Operator.

SIGNIFICANCE OF THE DISPLAY FUNCTION FIELD

UTIL Segment



Shows machine utility, ie. how much time the machine spends on level 0. As time spent on level 0 decreases, more display segments are lit.

HIT Segment



Shows how hit rate in cache. As HIT rate in cache increases, more segments are lit.

RING Segment



Paging off Ring 0 Ring 1 Ring 2 Ring 3

MODE Segment



Interrupt and paging system on.



Interrupt system on.

MONITOR FUNCTIONS (Also shown on DISPLAY)

Memory:

- E ↙ Set Physical Examine mode (default after MACL).
xE ↙ Set Virtual Examine mode. Map via page table x.
xxxxxxx/nnnnnzzzz ↙ Examine and change contents of memory address x from n to z. X is 24 bits at Physical and 16 bits at Virtual Examine.
xxxxxx < yyyyyy ↙ Dump contents of memory from address x to address y. Select 64K area of last examine.

Registers:

- xxRy/nnnnzzzz ↙ Examine and change contents of register Ry on level xx from n to z. Ry may be written as R0 = S, R1 = D, R2 = P, R3 = B, R4 = L, R5 = A, R6 = T, R7 = X.
xx < yyRD ↙ Dump registers R0 to R7 from level x to level y.
U/nnnnn Display Contents of User Register.
OPR/nnnnzzzz ↙ Change Operator's Panel Switches from n to z.

Internal Registers:

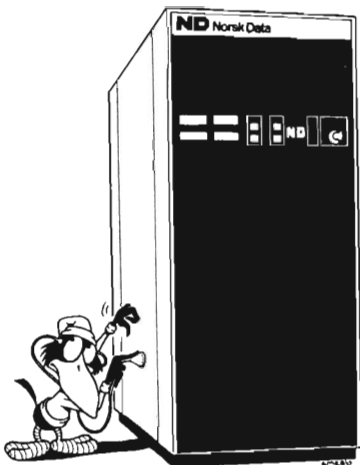
lxx/nnnnn Display Contents of Internal Register No. x.

x (4 bits): 0 = PANS 1 = STS 2 = OPR
 3 = PGS 4 = PVL 5 = IIC
 6 = PID 7 = PIE 10 = CSR
 11 = ACTL 12 = ALD 13 = PES
 14 = PGC 15 = PEA

lyy/nnnnzzzz ↙ Deposit z in Internal Registers No. y (n is dummy)

y (4 bits): 0 = PANC 1 = STS 2 = LMP
 3 = PCR 5 = IIE 6 = PID
 7 = PIE 10 = CCLR 11 = LCIL
 12 = UCIL 15 = ECCR

- IRD ↙ Dump Internal Registers 0 - 15 (only in STOP)
xx < yyRDE ↙ Dump Scratch Registers from level x to level y



Olaf Helsets vei 5,
P.O.Box 25, Bogerud,
N-0621 OSLO 6, NORWAY
Tel.: +47 2 29 54 00